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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,806	05/13/2002	Christian Paulus	32226.18	7278

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,806	PAULUS ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show "the at least one input node for the input signal is connected to the at least one evaluation circuit" in claim 3. In figure 3 that is a detailed drawing of claim 1, the input is not connected to the evaluation circuit (40, 41).

Figure 1 and figure 3 are objected to because the details in two drawings are not compatible. For instance, in figure 1, the evaluation circuit (50) receives signal (13) and the output signal from the output node (12). In figure 3, the evaluation circuit (50) receives only one input signal from node (12). Figures 1 and 2 are objected to because functional labels of the boxes are missing.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitations "at least one input node", "the input node" in claim 1, "at least one control transistor" in claim 8, "one regulating transistor" in claim 16 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 14 is objected to because the recitation" the drive strength" lacks antecedent basis.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "the first inverter stage being short-circuited with the input node" is indefinite because it is misdescriptive. By definition a short circuit is an abnormal connection of relatively low resistance between two points of the circuit. The result is a flow of damaging current between these two points. In figure 3 of the present application, the inverter (53, 54) is not short–circuited to the "input node". The Applicant is requested to point out in figure 3 the first and second inverters and the " input node". The connection of the second inverter (56, 57) to other components is not described in the claim.

Regarding claim 3, the recitation "at least one input node for the input signal is connected to the at least one evaluation circuit" is indefinite because it is misdescriptive. Figure 3 of the present application shows that the "evaluation circuit (50) is not connected to any "at least one input node". The Applicant is requested to show in the drawing the "at least one input node" and the recited connection.

Regarding claim 6, the recitation " the valuation circuit(s) is/are **at** low impedance" is indefinite because it is misdescriptive. The " valuation circuit in figure 3 of the present application comprises MOS transistors and it is well known that the MOS transistors are high input impedance devices. The Applicant is requested to prove that the evaluation circuit is a low impedance and show which input node is at low impedance. It is also not clear as to the input node of the valuation circuit has a "low input impedance" or a "low impedance" is connected to the input of the valuation circuit.

Regarding claim 12, the recitation "wherein a low-harmonics current is generated in the driver circuit" is indefinite because it unclear how a low-harmonics current can be generated by the driver circuit. Explanation is required.

Regarding claim 13, the recitation "a $\sin^2$-shaped current is supplied to the load" is indefinite because it is unclear how the output signal can be the square of the sine wave. Explication is required.

Claims 12-15 are rejected because they are method claims that depend upon an apparatus claim (claim 1).

Regarding claim 15, the recitation " the present edge steepness is measured by the at least one feedback capacitor" is indefinite because it is unclear how a capacitor can measure the "present edge steepness" of a signal. The capacitor can store a charge but it cannot perform the measurement (slew) of a signal. Explanation is required.

Claim 16 is rejected because it depends simultaneously upon an apparatus claim (claim 1) and a method claim (claim 12).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 7, 8,and 12-16, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Friedman et al. (US Pat. 6,163,174).

Regarding claim 1, figure 5 of Friedman shows a driver circuit, having, at least one input node for an input signal (Vin) and at least one output node for an output signal (Vout), having one or more, preferably two, sub-drivers (n6, Ib1-Ib5) and having a feedback circuit (CL, 19, I1D-I4D), which has one or more evaluation circuits (19) and one or more feedback capacitors (CL), the valuation circuit(s) (19, I1D-I4D), being connected to the sub-driver(s) and the feedback capacitor(s) (CL) respectively being provides between an output node (Vout) of the driver circuit and an input node of an evaluation circuit (the input of 19), the at least one evaluation circuit having a first inverter stage I1D) coupled to the input node of the valuation circuit , and also a second inverter stage (I2D), connected in series with the first inverter.

Regarding claim 2, the " at least one input" (Vin +) is connected to the "sub-driver" (via (19). The input (Vin-) is connected to the sub-driver (p6, I1a-I5a).

Regarding claim 3, the "at least one input node" is connected to the "at least one evaluation circuit (19, I1D-I4D).

Regarding claim 6, insofar as understood, the input node of the valuation circuit is at high input impedance (the input of the inverter circuit; see US Pat. 6,329,846, col. 5, lines 15-17).

Regarding claim 7, figure 5 shows that the sub-drivers (Ib1-Ib6) has more than one transistor.

Regarding claim 8, the control transistor (p1) of the sub-driver (I1b-I6b) is connected to the valuation circuit (19, I1D-I4D).

Regarding claims 12 and 13, it is inherent that a sine-wave input current with low harmonic current-content is inputted to the driver circuit, a sine-wave with low harmonic current is generated and the edge steepness (slew) is independent on the components of the driver circuit.

Regarding claim 14, in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated and the "drive strength" is "regulated" based on the "valuation result".

Regarding claim 15, the feedback capacitor (CL) varies the steepness of the output signal. The output signal of the valuation circuit (19, I1D-I4D) control at least one regulating transistor (m22, m32, m42, m52) for regulating the driver strength of the subdriver.

Regarding claim 16, the recitation " for improving the electromagnetic compatibility of electronic component" is merely "result" language and thus cannot be relied upon to distinguish over the disclosure of Friedman, since the reference meets all of the claimed structure (and the functions performed by that structure), the reference meets claim 16 under 102(b). Note that apparatus claims, to be patentable over the prior art, must define over the prior art by structure, not the result of that structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friedman et al. (US Pat. 6,163,174).

Regarding claim 9, figure 5 of Friedman includes al the limitations of claim 9 except for the limitation that the feedback capacitor is designed as a linear capacitor. However, it is old and well known in the art that a linear capacitor is fabricated using two polysilicon deposition steps in which polysilicon comprises both plates of the capacitor and it is highly desirable to implement a semiconductor process suitable for fabricating reliable and linear capacitors that can be integrated into an existing or base line CMOS fabrication process without adding cost in the form of additional processing. Therefore, it would have been obvious for those skilled in the art to replace the capacitors of Friedman with linear capacitors for cutting fabrication cost.

Regarding claim 10, figure 5 of Friedman includes al the limitations of claim 10 except for the limitation that the feedback capacitor is designed as a non-linear capacitor. However, it is old and well known in the art that a non-linear capacitor is simple a MOS gate capacitor. Therefore, it would have been obvious for those skilled in the art to replace the capacitors of Friedman with non-linear capacitors for cutting fabrication cost.

Regarding claim 11, the non-linear capacitors are formed using PMOS and NMOS transistor (well known).

Regarding claims 12 and 13, it is inherent that a sine-wave input current with low harmonic current-content is inputted to the driver circuit, a sine-wave with low harmonic current is generated and the edge steepness (slew) is independent on the components of the driver circuit.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ten Eyck (US Pat. 6,137,322).

Regarding claim 1, figure 2 of Eyck shows a driver circuit, having, at least one input node (36) for an input signal and at least one output node (68) for an output signal, having one or more sub-drivers (32, 23, 24, 26, 27, 54, 57, 59) and having a feedback circuit (63, 65, 58), which has

one or more evaluation circuits (63, 65), the valuation circuit(s) being connected to the sub-driver(s) and an output node (68) of the driver circuit, the at least one evaluation circuit having a first inverter stage (65) coupled to the input node of the valuation circuit , and also a second inverter stage (63), connected in series with the first inverter stage except for the limitation that there is a feedback capacitor connected between the output node of the driver (68) and the input of the first inverter (65). However, it is old and well known in the art that the capacitor coupled between the output of a circuit and the input of the other circuit for blocking the DC component of the output signal. Therefore, it would have been obvious for those skilled in the art to implement a "feedback capacitor" between the output (68) of the driver and the input of the first inverter (65) for the purpose of blocking the DC component of the output signal for preventing the premature triggering of the feedback circuit.

Regarding claims 2 and 3, the input node (36) is connected to element (32) of the subdriver. The input node (36) is connected to the evaluation circuit (63, 65) element (32, 26, 56, 57).

Regarding claim 4, the second sub-driver is (20, 21, 29, 30, 50, 51, 60).

Regarding claim 5, the second feedback circuit (52, 62, 64), like the feedback circuit in claim 1, a "feedback capacitor" will be implemented between the output (68) of the driver and the input of the first inverter (64) for the purpose of blocking the DC component of the output signal for preventing the premature triggering of the feedback circuit.

Regarding claim 6, insofar as understood, the input node of the valuation circuit is at high input impedance (the input of the inverter circuit; see US Pat. 6,329,846, col. 5, lines 15-17).

Regarding claim 7, the sub-driver has more than one transistor.

Regarding claim 8, the control transistor (54 or 57) is connected to the evaluation circuit (63, 65).

Regarding claim 9, as mentioned above, the linear capacitor is used cutting fabrication cost.

Regarding claim 10, as mentioned above, the non-linear capacitors for cutting fabrication cost.

Regarding claim 11, the non-linear capacitors are formed using PMOS and NMOS transistor.

Regarding claims 12 and 13, it is inherent that a sine-wave input current with low harmonic current-content is inputted to the driver circuit, a sine-wave with low harmonic current is generated and the edge steepness (slew) is independent on the components of the driver circuit.

Regarding claim 14, in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated and the "drive strength" is "regulated" based on the "valuation result".

Regarding claim 15, the feedback capacitor varies the steepness of the output signal. The output signal of the valuation circuit (58, 63, 65) controls at least one regulating transistor (54, 57) for regulating the strength of the driver circuit.

Regarding claim 16, the recitation " for improving the electromagnetic compatibility of electronic component" is merely "result" language and thus cannot be relied upon to distinguish over the disclosure of Friedman, since the reference meets all of the claimed structure (and the functions performed by that structure), the reference meets claim 16 under 102(b). Note that apparatus claims, to be patentable over the prior art, must define over the prior art by structure, not the result of that structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
Examiner
02-03-2003

TUAN T. LAM
PRIMARY EXAMINER